CLAIMS

1. A process for fabricating an integrated circuit, comprising the production of several metallization levels, which are mutually separated by interlevel insulating layers, and of intertrack insulating layers each separating the tracks of the same metallization level, and the production of at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the production of the capacitor comprises:

the simultaneous production, in at least part of an intertrack insulating layer associated with a given metallization level, on the one hand, of the two electrodes and of the dielectric layer of the capacitor and, on the other hand, of a conducting trench which laterally extends the lower electrode of the capacitor, is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor; and

the production, in the interlevel insulating layer covering the intertrack insulating layer, of two conducting pads which come into contact with the upper electrode of the capacitor and with the conducting trench, respectively.

2. The process according to Claim 1, wherein the trench comprises only the conducting material forming the first electrode.

3. The process according to Claim 1, wherein the tracks of the given metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

4. The process according to Claim 1, wherein the production of the capacitor and of the trench comprises:

a) the formation of the intertrack insulating layer on an interlevel insulating layer;

b) the etching of at least part of the intertrack insulating layer so as to form a cavity having a main part laterally extended by the trench;

c) the formation of a first layer of a first conducting material on the structure obtained in step b) and the formation of a layer of a dielectric on the first layer;

d) the formation of a second layer of a second conducting material on the dielectric layer so as to fill the main part of the cavity, the dimensions of the trench and the thicknesses of the first layer and of the dielectric layer being chosen so as to obtain, after step d), a trench comprising at least the first conducting material but not containing the second conducting material; and

e) chemical-mechanical polishing of the multilayer stack formed in steps c) and d) so as to leave, in the main part of the cavity, the capacitor whose lower electrode is formed from a residual part of the first layer coating the internal walls of the cavity and whose upper electrode is formed from a residual part of the second layer, which is separated from the residual part of the first layer by a residual part of the dielectric layer, and to leave, in the trench, another residual part of the first layer coating at least the internal walls of the trench, to the exclusion of any residual part of the second layer.

5. The process according to Claim 4, wherein the trench comprises only the conducting material forming the first electrode.

6. The process according to Claim 4, wherein the tracks of the given metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

7. The process according to Claim 4, wherein the production of the tracks of the given metallization level comprises:

after step c), etching of the dielectric layer, of the first conducting layer and of the intertrack insulating layer so as to form at least one auxiliary trench;

the deposition of the second conducting layer carried out in step d) so as to fill the trench or trenches; and

the chemical-mechanical polishing carried out in step e) so as to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

8. The process according to Claim 4, wherein the first conducting layer and the dielectric layer are formed in step c) by a conformal coating and in that the width of the trench is at least twice the thickness of the first conducting layer and less than twice the sum of the thickness of the first conducting layer and of the thickness of the dielectric layer.

9. The process according to Claim 8, wherein the trench comprises only the conducting material forming the first electrode.

10. The process according to Claim 8, wherein the tracks of the given metallization level are produced simultaneously with the formation of the upper electrode of the capacitor.

11. The process according to Claim 10, wherein the production of the tracks of the given metallization level comprises:

after step c), etching of the dielectric layer, of the first conducting layer and of the intertrack insulating layer so as to form at least one auxiliary trench;

the deposition of the second conducting layer carried out in step d) so as to fill the trench or trenches; and

the chemical-mechanical polishing carried out in step e) so as to remove the first conducting layer, the dielectric layer and the second conducting layer from the surface of the intertrack insulating layer.

12. An integrated circuit comprising several metallization levels, which are mutually separated by interlevel insulating layers, and intertrack insulating layers each separating the tracks of the same metallization level, and at least one capacitor comprising a lower electrode and an upper electrode which are mutually separated by a dielectric layer, wherein the capacitor is located in at least part of an intertrack insulating layer associated with a given metallization level, in that the lower electrode of the capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and in that the integrated circuit comprises, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads which come into contact with the upper electrode of the capacitor and with the conducting trench, respectively.

13. The integrated circuit according to Claim 12, wherein the tracks of the given metallization level are formed from the material as that forming the upper electrode of the capacitor.

14. The integrated circuit according to Claim 12, wherein the trench comprises only the conducting material forming the lower electrode.

15. The integrated circuit according to Claim 14, wherein the tracks of the given metallization level are formed from the material as that forming the upper electrode of the capacitor.

16. The integrated circuit according to Claim 12, wherein the trench comprises only the dielectric encapsulated by the conducting material forming the lower electrode.

17. The integrated circuit according to Claim 16, wherein the tracks of the given metallization level are formed from the material as that forming the upper electrode of the capacitor.

18. An integrated circuit comprising:

a plurality of metallization levels that are mutually separated by interlevel insulating layers, and intertrack insulating layers each separating the tracks of the same metallization level; and

at least one capacitor comprising a lower electrode and an upper electrode, which are mutually separated by a dielectric layer, and wherein the capacitor is located in at least part of an intertrack insulating layer associated with a given metallization level, in that the lower electrode of the capacitor is laterally extended by a conducting trench, which is electrically isolated from the upper electrode and has a transverse dimension smaller than the transverse dimension of the capacitor, and wherein, in the interlevel insulating layer covering the intertrack insulating layer, two conducting pads come into contact with the upper electrode of the capacitor and with the conducting trench, respectively, and wherein the tracks of the given metallization level are formed from the material as that forming the upper electrode of the capacitor.

Sub G4